HITACHI KP-M1 Sensor (CCIR) ICX024BL-3

Interline-type CCD Image Sensor

Description

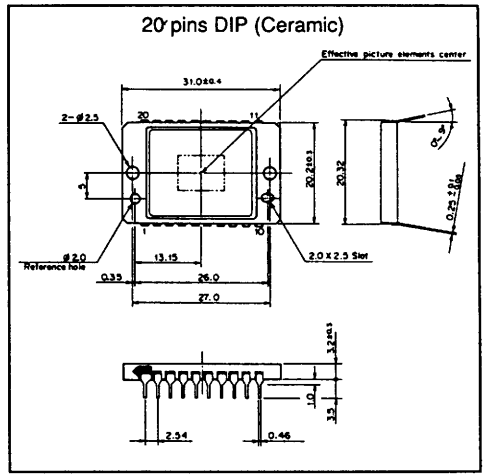
ICX024BL-3 is an interline-type CCD image sensor for B/W video cameras designed for the CCIR system.

Effective pixels number 756 horizontally and 581 vertically.

Field integration read out method ensures high dynamic resolution.

Package Outline

Unit: mm



Features

- Image size: 2/3 inches (8.8 mm(H) × 6.6 mm(V))
- Effective pixels: 756 (H) × 581 (V)
- Effective optical black
  - Horizontal: Front 5 pixels
    Back 55 pixels
  - Vertical: Front 19 pixels
    Back 6 pixels
- High resolution, high sensitivity and low noise.
- Low lag and low smear
- Low dark current
- Anti-blooming function
- Electronic shutter function
- Neither figure distortion nor microphonic noise.
- γ characteristics: 1

Element Structure

- Interline type CCD image sensor
- Chip size: 10.0 mm(H) × 8.2 mm(V)
- Unit cell size: 11.0 μm(H) × 11.0 μm(V)
- Dummy bits: horizontal 22-bits, vertical 1-bit (even field only)
- HAD (Hole Accumulation Diode) Sensor

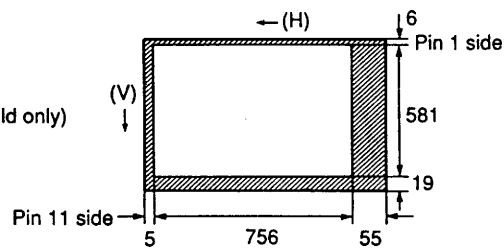
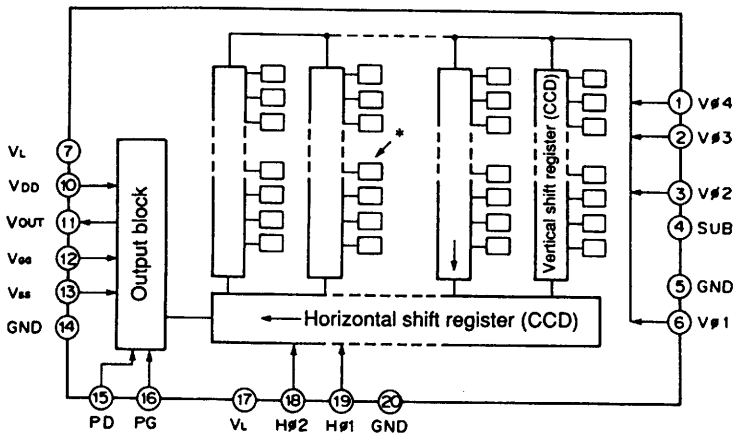


Fig. 1 Optical black configuration

Imaging Device Function Block and Pin Configuration



Pin Description

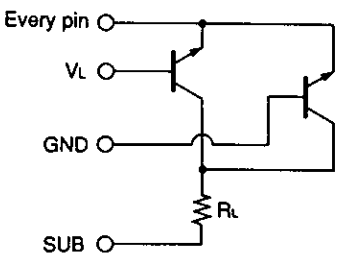
No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	Vφ1	Vertical register transfer clock	16	PG	Output reset clock
7	VL	Protective transistor bias	17	VL	Protective transistor bias
8	NC		18	Hφ2	Horizontal register transfer clock
9	NC		19	Hφ1	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
Between SUB and GND	−0.3 to +5.5	V	
Between each of V_{DD}, PD, V_{OUT}, V_{SS} and GND	−0.3 to +20	V	
Between each of V_{DD}, PD, V_{OUT}, V_{SS} and SUB	−55 to +10	V	Note 1
Between each of Horizontal and vertical transfer clock inputs and GND	−15 to +20	V	
Between each of Horizontal and vertical transfer clock inputs and SUB	−65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	15	V	Note 2
Potential difference between horizontal transfer clock inputs	17	V	
Between each of $H\phi_1$, $H\phi_2$ and $V\phi_4$	−17 to +17	V	
Between each of PG, V_{GG} and GND	−10 to +15	V	
Between each of PG, V_{GG} and SUB	−55 to +10	V	Note 1
Between V_L and SUB	−65 to +0.3	V	
Between pins other than GND, SUB, V_L and V_L	−0.3 to +27	V	
Storage temperature	−30 to +80	°C	
Guarantee operational ambient temperature	−10 to +55	°C	

Note) 1. This image sensor consists of an N-type substrate P-Well structure where a protective transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V. The series resistance R_L must be more than 1 kΩ between V_{DD} and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5 kΩ between V_{SS} or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5kΩ.

1) V_{DD}, PD, V_{OUT} and V_{SS} pins



2) Pins other than 1) (except V_L and GND)

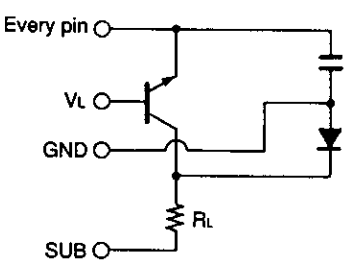


Fig. 2 Equivalent circuits

2. In case clock width is as follows: <10 µs and clock duty factor <0.1%, up to 27 V is guaranteed.

Electrical Characteristics

Bias conditions

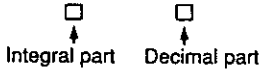
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	Note 1
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5%
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	−3		3	%	
Protective transistor bias	V_L	To be the vertical transfer clock low-level clamp bias				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.
V_{SUB} code – Two digits indication



The integral code corresponds to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Numerical value	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground V_{SS} with a 390 Ω resistance

4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Ground all pins other than those under test.
2) Current flowing to the ground when a voltage of 20 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply a voltage of 20 V to the SUB pins and ground pins other than those under test.
3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.

5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.

Clock Voltage Conditions
Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	−0.5		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	−10.5			V	
Horizontal transfer clock voltage	V_{HHH}			5.2	V	Note 3
	V_{HL}	−3.0		−1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	−3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between output reset clock and GND	$C_{\phi PG}$		10		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		500		pF	

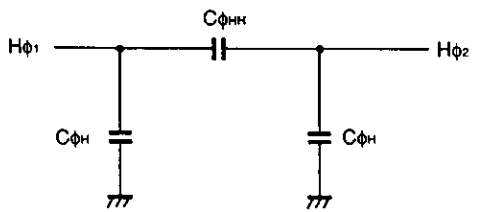


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_2$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at $V\phi_1$) and "V_{T3}" (at $V\phi_3$). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

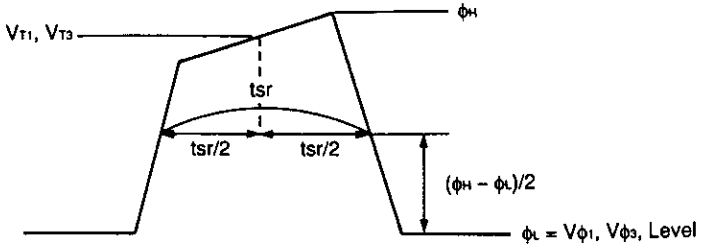


Fig. 5 Read clock wave form

2. Vertical clock voltage (Refer to Fig. 6)

T = 564 ns (with a horizontal driving frequency of 14.19MHz)

1) Definition of the vertical transfer clock amplitude

Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_2$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ Level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ Level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ Level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi V$".

2) The maximum value among V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in $V\phi_1$ and $V\phi_3$ only).

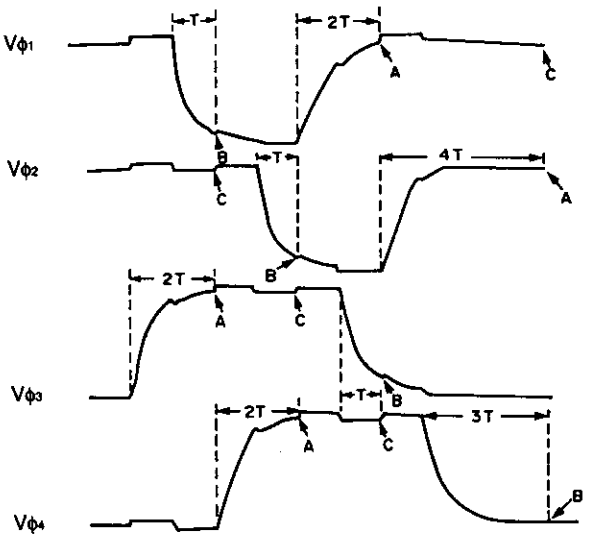


Fig. 6 Vertical transfer clock waveform

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".

   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
   And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

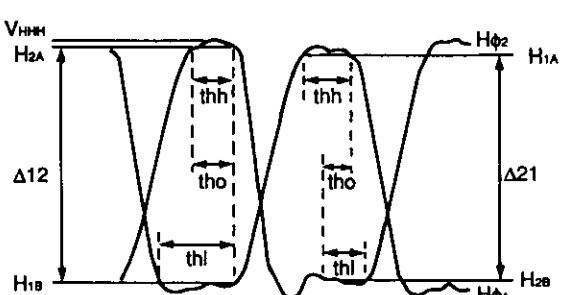


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

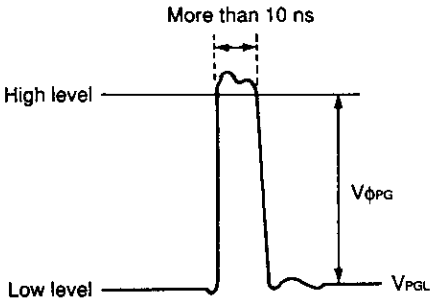


Fig. 8 PG clock waveform

5. Substrate clock voltage
   1) Substrate voltage is expressed as ϕ_L and the maximum value of the substrate clock waveform as ϕ_H.
   2) The period during which voltage level reaches $(\phi_H - \phi_L)/2$ is expressed as tsr. The difference of voltage level with ϕ_L at tsr/2 is defined as substrate clock voltage $V\phi_{SUB}$.

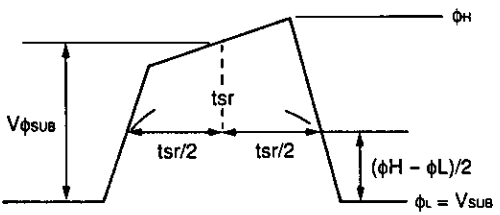


Fig. 9 Substrate clock waveform

Driving Clock Waveform Conditions

1) Definition of ϕ_H (100%) and ϕ_L (0%)
   (1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock ($PG\phi$) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   (2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_3$) is applied.
   (3) For the substrate clock ($SUB\phi$), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".
2) Standard driving clock waveform conditions (Typ.)

Horizontal drive frequency: 14.19MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
$H\phi_1$	18	33.7	10	8	ns	Imaging period
$H\phi_2$	18	33.7	10	8		
$H\phi_1$	4.9		0.10	0.01	µs	Parallel-serial converting period
$H\phi_2$		4.9	0.10	0.01		
ϕ_{PG}	12	53.7	2	2	ns	
$V\phi_1/V\phi_2$	61.6	1.6	0.1	0.1	µs	Imaging period
$V\phi_3/V\phi_4$	2.8	60.45	0.05	0.1		
$V\phi_T$	2.4		0.2	0.1		Reading period
SUBϕ	1.0		0.08	0.1	µs	Electron sweep-off period

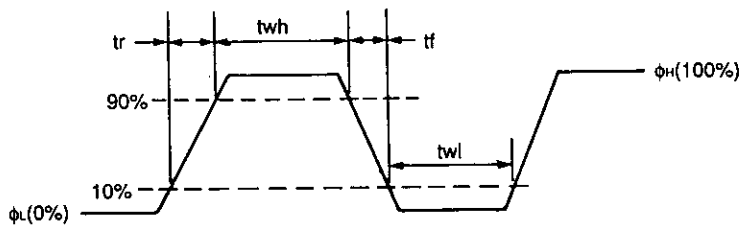


Fig. 10 Clock waveform

Imaging Characteristics

(For the testing circuit, see Fig. 11.)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sg	200	300		mV	1	
Output saturation signal	Vsat	500			mV	2	Note
Blooming margin		800			times	3	Note
Smear	Smr		0.005	0.012	%	4	
Video signal shading	Svg			20	%	5	
Dark signal output	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C

Note) Saturation signal and blooming margin are guaranteed only when the substrate voltage has been set to the voltage indicated on the back of the imaging device.

Test Methods

Conditions

1) The conditions required to drive the device through out the following tests should be within the range of bias conditions and clock voltage conditions. The test circuit shown in Fig. 11 is used for evaluating and testing the characteristics.
2) Blemishes are excluded in the following tests and the signal output is based on the optical black level unless otherwise specified. The value obtained at the output test point becomes the test value.

Standard Imaging conditions

1) Shoot the PTB-100 pattern box (luminance 706 Nit, color temperature 3200K) with no pattern, using a FUJINON H6 x 12.5D (F1.4) lens at F8. Use the CM-500S (1.0 mmt) filter to cut off infrared rays.
2) Shoot a light source (color temperature 3200K) which provides a uniform brightness within 2% over the whole screen.

1. Set the standard imaging condition 1) and test signal voltage (Sg) at the center of the screen.

2. Set to standard imaging condition 2) and adjust the light intensity to about eight times the intensity obtained at a signal voltage of 200 mV. Them obtain the minimum value of the signal voltage over the whole screen.

3. Set to imaging condition 2) and adjust the light intensity to about 800 times the intensity obtained at a signal voltage of 200 mV. At that time make sure there is no blooming and the vertical resistor is not saturated.

4. Set to standard imaging condition 2) and adjust the light intensity so that the signal voltage (V_{SG}) becomes 200 mV. Then, turn V_T off and obtain the maximum value of the signal voltage "V_{SM}" after stopping the horizontal resistor 50 H at the effective picture element.

$$Smr = \frac{V_{SM}}{V_{SG}} \times \frac{1}{50} \times \frac{1}{10} \times 100\ (\%)$$

(Converted into 1/10 V system)

5. Set to standard imaging condition 2) and test the signal voltage to obtain maximum (V_{SG} max) and minimum (V_{SG} min) values.
The light intensity is adjusted so that the average value of the signal voltage (V_{SG} average) becomes about 200 mV.

$$Svg = \frac{V_{SG}\,max - V_{SG}\,min}{V_{SG}\ average} \times 100\ (\%)$$

6. Measure the mean voltage of the dark current signal based on the horizontal free-transfer level in a light-shaded condition with an ambient temperature of 55°C.

7. Following measurement 6, test the dark current signal voltage to obtain the maximum (Vdmax) and minimum (Vdmin) values. Spot blemishes are ignored in this test.

Electrical Characteristics Test Circuit

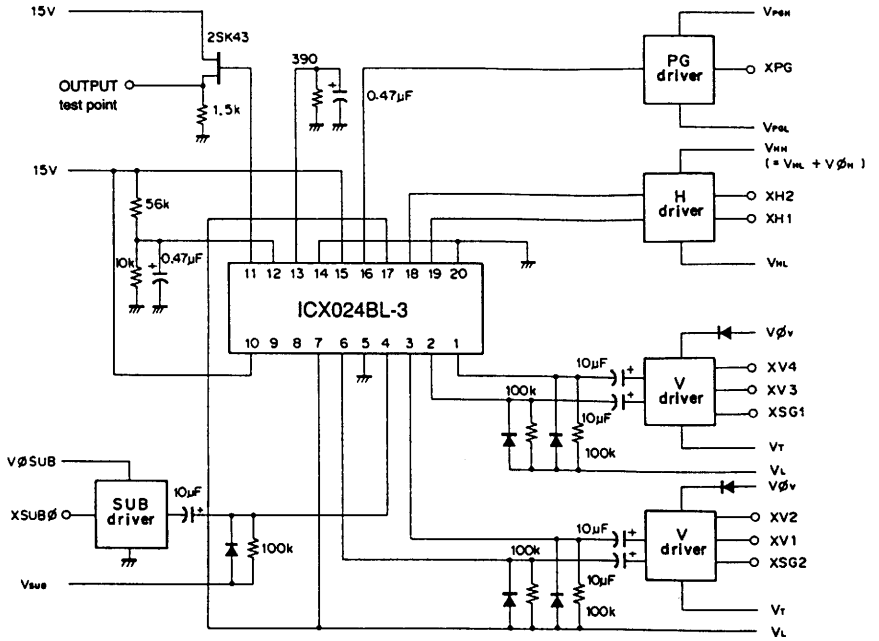
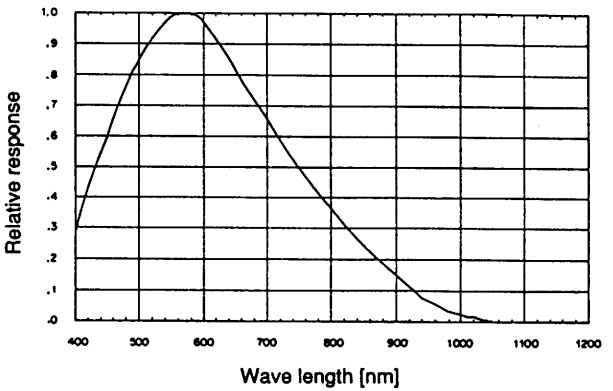


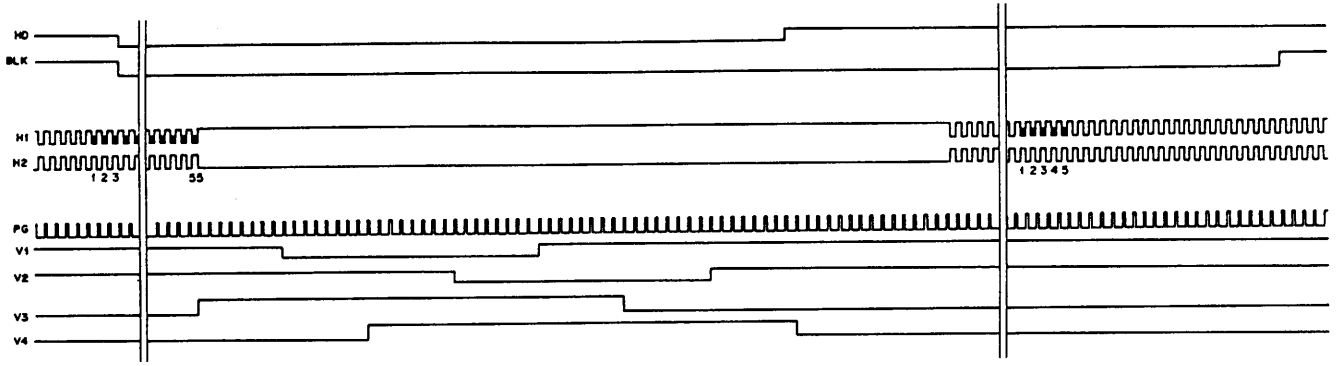
Fig. 11

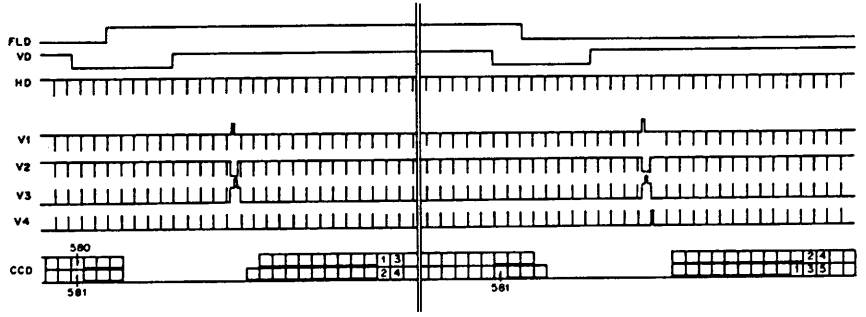
Spectrum Sensitivity Characteristics (Typical example, excluding illuminant characteristics)

With a Fujinon lens H6 × 12.5D

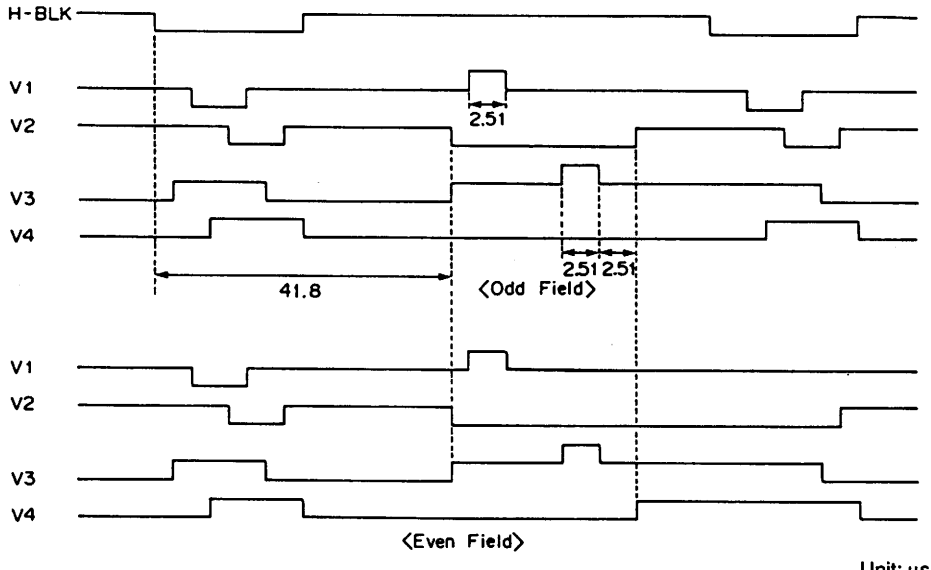


Driving Pulse Timing Chart



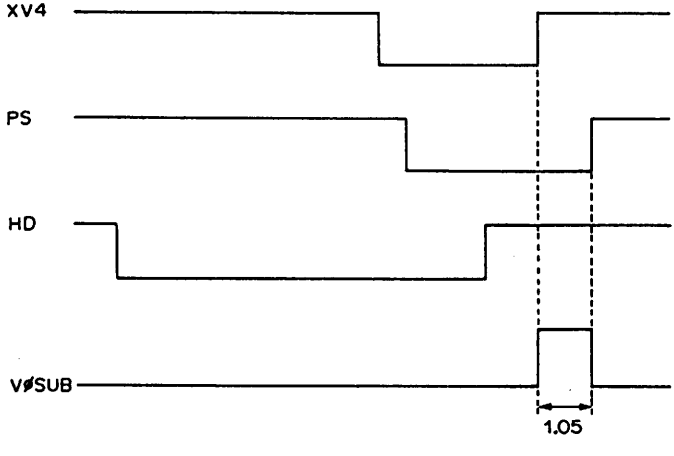


Sensor Read Out Clock Timing Chart



Unit: µs

Charge Drain Clock Timing Chart in Shutter Mode



Unit: µs

Handling Instructions

1. On electric screening
   To prevent damage to the CCD image sensor by static electricity, handle as follows.
   a) Either handle the device with bare hands, or use antistatic gloves and clothes. Conductive shoes are also required.
   b) Use a ground lead when directly touching the device.
   c) Cover the floor and working table with a conductive mat or equivalent to avoid static electricity.
   d) Discharge using ionized air is recommended.
   e) To ship the mounted boards, use cartons with antistatic properties.

2. On soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder-dipping of DIP in a mounting furnace may break glass. Use a grounded 30 W soldering iron at each pin for less than 2 seconds. When adjusting or removing soldered parts, let the CCD cool sufficiently.
   c) Do not use any solder-aspirating equipment to remove the imaging device. Should an electric solder-aspiration device be used, use only a device of the zero-cross type control system and be sure to ground the controller.

3. On contamination
   a) Keep the operation room clean (Class 1000 will be expected).
   b) Do not touch the glass surface and avoid contact with foreign objects. Blow off any dust from the surface with a blower. (Ionized air is recommended to blow off any object sticking through static electricity.)
   c) Wipe off grass spots with an applicator moistened with ethanol. Be careful not to scratch the surface.
   d) To eliminate contamination, store the device in an exclusive case. During transportation minimize the difference in temperatures between locations to avoid moisture condensation.
   e) When a protection tape has been affixed for shipment, remove it just before use after applying appropriate antistatic measures. Do no reuse the removed tape.

4. Do not subject the device to light sources for extended periods. If a color element is subjected to strong light ray for an extended period, the color filter will be discolored. (Store the device in a dark place.)

5. Usage or storage of the device in high temperature or high humidity may seriously affect the performance.

6. The CCD image sensor is a high-precision optical part, that should not be subjected to mechanical shocks.

7. System data write complete ROM (with flow compensation address included)
   System data write complete ROM in equal quantity as ICX024BL-3 is attached.
   Analog those ROM with address for flow compensation have serial No. stuck on.
   Use in conjunction with ICX024BL-3 pairing the same serial No..

Spectrum Sensitivity Characteristics (Typical example, excluding illuminant characteristics)

With a Fujinon lens H6 × 12.5D